QCA based Novel Reversible Reconfigurable Ripple Carry Adder with Ripple Borrow Subtractor in Electro-Spin Technology

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ABSTRACT

An important arithmetic component of "Arithmetic and Logic Unit" or ALU is reconfigured in this paper, known as "Full-Adder-Subtractor", where an advance low-power, high-speed nano technology "QCA" with electro-spin criterion is used with reversibility and the advancement of multilayer 3D circuitry. In this modern digital world, this selected nano-sized technology is an effective alternative of widely used "CMOS Technology" because all the limitations, mainly limitation due to the presence of high power dissipation at the time of device-density increment in a "CMOS" based integrated circuit, can be optimized by "QCA" nano technology with electro-spin criterion and this technology also supports reversible logic in multilayer 3D platform with less complexity. This paper, primarily presents two novel "QCA" based 3-layered "Adder-Subtractor" designs using the collaboration of multilayer inverter gates, reversible modified 3-input Feynman-Gate and 3-input MG (Majority Gate) with very less cell-complexity, area-occupation, delay and energy-dissipation and high output-strength, temperature-tolerance and accuracy. A clear parametric investigation on presented designs are shown clearly in this paper through a comparative manner with some previous published related structures. Additionally, another parametric-experiment on a novel multibit reversible multilayer "QCA" based "Full-Adder-Subtractor" circuitry using the working phenomenon of "Ripple Carry Adder" (RCA) and multibit subtractor ("ripple borrow subtractor" or RBS) is presented in this proposed work in a proper way and this combination of RCA and multibit subtraction operation converts the proposed circuitry into a hybrid form, which is more effective compare to some other advanced adders in parametric-optimization field.

Keyword

Electro-Spin, Hybrid, QCA, Reversibility, Ripple Carry Adder, Ripple Borrow Subtractor

Introduction

In this advance nano-technical digital world ALU or "Arithmetic and Logic Unit" is a key component of any processor and Full-Adder is an important component of ALU [8] as a part of the arithmetic unit. Design a novel advanced circuitry of this full-adder with the addition of full-subtractor is the main motive of this paper. Till now, "CMOS Technology" is used to design this proposed circuitry, because this technology effectively follows "Moore's Law" [1] to design high dense integrated-circuit and according to this law the number of used transistors in a dense integratedcircuit is doubled for every two tears. But, when the area is reduced of these highly dense integrated-circuits, there are several limitations take place, such as design-complexity increment, delay increment due to this complexity, energydissipation increment due high leakage current flow etc. Thus, the requirement of an advance low-power, high speed nano-technology becomes very important and proposed "QCA" technology [3-5] with electro-spin criterion can fulfill all these above requirements at the time of any logical device implementation, which is introduced by Tougaw and Lent et.al in 1993 [2]. After that time, various types of combinational and sequential representations are experimented in this "QCA" platform till now. There are also

various types of "OCA" based designs on full-adder, fullsubtractor or full-adder-subtractor are already published in different articles in different years [9-15] and the parametricoptimization of proposed component is rapidly increased in last few years. In 2017, Barughi and Heikalabad presented a "Full Adder/Subtractor" design using 90 quantum cells in a multilayer 3D platform, where 3 layers are required with 0.6 μ m² area and 1.5 clock-cycle delay [11] and this occupied area $(0.14 \ \mu m^2)$ and delay $(1.25 \ clock-cycle)$ are reduced by Firdous Ahmad et.al in the next year, where the reversible gates (3:3 New Reversible Gate and Modified Feynman Gate) are used to design the published structure with proper powerdissipation calculation. But, in that design the quantum cell number is increased up to 121 cells in single layer "QCA" platform [12]. To minimize this problem, two different structures of full adder and subtractor are formed by Md. Abdullah-Al-Shafi et.al [13], which are published after 3 months of the previous work acceptance. If those two designs are combined in a multilayer platform, then only 49 cells are required to design the "Adder-Subtractor" device with 2 clock-zone latency and 0.04 µm² occupied area. In our proposed full-adder-subtractor design, the device-occupiedarea, delay, energy-dissipation and quantum-cost are

minimized compare to other previous published structures. The cell-count of proposed circuit is reduced more by Moein Sarvaghad-Moghaddam et.al in 2019 [14], which is formed to design 8 bit reversible "Adder/Subtractor" design. In that above design, 2 to 1 MUX is added with reversible "Adder-Subtractor" design and in this paper the presented single-bit reversible "Adder-Subtractor" design is compared with our proposed multilayer reversible "Adder-Subtractor" design, which ultimately gives a multilayer multi-bit (4-bit) "Adder-Subtractor" design based on the combination of RCA and RBS (hybrid formation). In that "Adder-Subtractor" design of paper [14], 48 cells quantum cells are required, where the occupied area is 0.039 μ m² and delay is 3 clock-zone and 2 garbage outputs are present in that proposed design which is reduced in our design by using them as the inputs of fullsubtractor. These parameters are again optimized in next year down to 38 cells, 0.03 µm² area and 0.5 clock-cycle (2 clockzone) delay by Mostafa Sadeghi, Keivan Navi et.al [15] in multilayer platform with proper energy dissipation calculation. The discussed recently published optimized "Adder-Subtractor" structure is an irreversible structure. But presently, the improvement of "QCA" based logical structures becomes a big challenge. Thus, in this paper, reversible gate is chosen in multilayer platform to bring more advancement of our proposed "Adder-Subtractor" physicalformation and this multibit design of proposed advanced adder with subtraction operation is more acceptable than other advanced adder circuits, such as "Carry Look Ahead Adder" or CLA and "Carry Save Adder" or CSA [6] due to the better occupied-area, delay and energy-dissipation reduction capability of our proposed design compare to other discussed designs. This design also maintains the outputstrength effectively at high-temperature with high faulttolerance and low quantum-cost in multilayer 3D platform due to the presence of reversible gates, which follow the adiabatic logic [7].

1.00
Polarization = +1
-1.00
Polarization = -1

In this paper, the flow of proposed work-done is continued through some sections, in which the theoretical background of proposed technology and proposed logic, presented designs and getting outputs and parametric investigations are discussed one after another from section 2 to section 4 serially and finally, section 5 presents the conclusion and future scope of our proposed paper-work.

Background of Proposed Technology and Proposed Logic

Electro-Spin Criterion Based "QCA" Cell Configuration and Working Phenomenon

Electro-Spin criterion based "Quantum-Dot Cellular Automata" or "OCA" technology is mainly used to form physical level logical design of any combinational and sequential digital component in this nano-electronic era and these components become a useful alternative of "CMOS" based logical components, which is already discussed in the introduction part of this paper. This proposed advanced technology is a four quantum-dot based technology, where the quantum cells are placed one after another to form a quantum wire and information flow from input to output is possible over here by the interaction of neighboring quantum cells. The discussed four quantum-dots are specified in each quantum cell, where two dots are occupied by electron, which are placed at a diagonal way. When the electrons of quantumdots become excited, they start to move through tunnel in a spintronic direction and this electro-spin concept helps to flow information from one cell to another cell. The polarization of quantum-dot cells is another important factor of this proposed technology, which depends on this above concept. When electrons start to flow at a clock-wise direction, it is considered as a positive polarization means binary '1' and when the movement is in anti-clock wise direction the cell-polarization becomes negative means the quantum-dot cells are act as binary '0'.

1.00 Polarization = +1 -1.00 Polarization = -1

(a)

(b)

Figure 1. (a) The '90°' binary zero cell-design and binary one cell-design in QCA (b) The '45°' binary zero cell-design and binary one cell-design in QCA

Figure 1 (a) and (b) represent the binary zero and binary one cell-design (figure 1 is "90° cell-design" and figure 2 is "45° cell-design") where the two electrons are placed in two separate diagonal position due to the electrostatic repulsion between the same charged carriers (electrons).

"QCA" Gate Structure

In this section some important gates in QCA electro-spin technique are properly discussed, which are rapidly used to form any binary expression in the digital field. "90° quantum cells" are used in these presented gate designs due to get less energy-consumption [16] and higher

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output-amplitude level compare to " 45° rotated quantum cells". Three input majority gate (3-input MG), five input majority gate (5-input MG) and inverter gate are some rapidly utilized and most effective gates in this suggested advanced nano technology. The input polarity of 3-input MG is same as the output polarity of the same gate. Let, a, b and c are the three inputs of this above gate-structure then the output looks like equation.1. This gate also can be used to design 'AND' gate and 'OR' gate by changing the polarity (-1 and +1) of one of the used three inputs in three input majority gate, which are also given in equation. 2 and 3 respectively. The 3-input MG is presented below in figure 2 (a). In introduction part, it is clearly revealed that this proposed technology is mare advance than "CMOS

Technology". If in this part the "CMOS" designs of these above gates are compared to proposed "QCA" design, then it can be said that the number of used cells is less than the number of used transistors to form all those above gatestructures. Such as: more than 25 transistors are required to design 3-input MG and 6 transistors are required to design each 'AND' gate and 'OR' gate, where in proposed technical design, all these discussed gates can be presented through 5 number of quantum cells with less leakage current flow and less required power and dissipated power.

M(A, B, C) = AB + BC + CA(1)
M(A, B, 1) = AB + B.1 + A.1 = A + B(2)
M (A, B, 0) = AB + B.0 + A.0 = A.B (3)



Figure 2. (a) 3-input MG by using quantum-dot-cells. (b) 5-input MG by using quantum-dot-cells. (c) A basic inverter gate structure of QCA technology.

Table 1. Truth table of the 5-input MG				
Sum of (A, B, C, D, E)	Majority of (A, B, C, D, E)			
0	0			
1	0			
2	0			
3	1			
4	1			
5	1			

The 5-input MG with proper truth table is also presented in this part by using figure 2 (b) and table 1. As it is known that for any binary representation the 'NOT' gate plays an important component-role and it can be easily designed in "QCA" technology as an inverter gate. The above figure 2 (c) presents an inverter gate in single layer form, but when it is converted into multilayer form the number of used cells are 50% reduced with high output strength. This acts as another advantage of proposed discussed technology to form low power and low-sized digital logic-gates.

Clocking Phenomenon of Proposed Technology

The designs based on proposed "QCA" technology can be performed two ways of clocking-phenomenon. Such as: "zone-clocking" and "continuous-clocking". In "Zoneclocking" the change of the clock zone in a quantum path need to be changed the potential-barrier between quantumdots to get the propagation delay of output (which is directly proportional to the used clock-zones in a quantum-wire) [17]. Thus, the change of the clock-zones need to be controlled, because the wide change of clock-zones brings continuous change of barrier-potential, which can increase the power consumption and the power dissipation of the device also. An advance clocking scheme, named as "Bennett-Clock-Scheme" is already introduced in paper [18], where the information can be saved before erase, which can also reduce the amount of dissipated power/bit without compromising the reduction of delay of proposed design.

If we discuss about the basics of the clock-zones, then it is also an important topic to discuss about the four clock-phases of each clock-zone. These four clock-phases are switch, hold, release and relax, which are clearly represented over here in figure 3. In switch phase the cells are switched to work. Then,

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the hold phase helps to flow the information by electronspecification in the quantum dots based on the polarization of neighboring cells. In release phase a complete relocation of electrons take place and a complete relocation is possible in relax phase. 90° phase difference is fixed in this clocking scheme between two clock-phases.



Figure 3. "QCA" Clocking-Scheme

Basics of Reversible Gate



Figure 4. Block-Diagram of reversible gate.

Previously discussed "Bennet-Clock-Scheme" is effectively used for reversible logic, which follows adiabiticity to maintain the extra heat generation at the time of device-layerincrement takes place. This reversible logic-gate is used in this work to design an arithmetic unit and logic unit combination (important part of the core component, named as "Arithmetic and Logic Unit" or "ALU", of any digitalprocessor). In conventional gate only input-based outputs are achieved, but, in reversible gate inputs can also be represented by outputs and vice-versa [19]. A clear blockdiagram of a reversible gate is presented in this portion in figure 4. This figure clearly shows that the number of inputs and outputs of reversible gate need to be same and more than one logical representation can be performed by using a single reversible logic-gate. It can reduce the area, delay and complexity of design. Briefly it can be said that the advancement of selected "QCA" design can be explored by applying reversible logic [20].

Used Multilayer Structure



Figure 5. 3D Structure using multiple layers in "QCA" Design.

It is known that "QCA" technology is used to design integrated circuits, where it is very important to check the type of wire-crossing of the chosen design. The wire crossing in proposed "QCA" design can be possible in single layer as well as, multilayer 3D formation. In single layer formation, wire crossing takes place by the crossing of "90° and 45° quantum cells". But, sometimes it brings huge complexities in design-formation. Thus, another process is brought to the field, which is clock-zone base wire-crossing technique. In this wire-crossing technique, the crossing can be possible by "180° phase alternate". But, due to the change of the clockzone, the device-delay is also increased. Therefore, an advance wire-crossing is needed to get power-efficient, highdense and high-speed circuit easily. This multilayer wirecrossing process can form a 3D design by specifying different cells in different layers and a by using a connecter-layer between two different utilized layers.

The multilayer structural improvement of selected "QCA" technology with electro-spin criterion is utilized in this work, where three dimensional (3D) structure (presented in this paper in figure 5) can be formed from two dimensional (2D) structure for unit-area and delay reduction and multilayer 3D inverter gates are used to form the proposed components with 18 nm quantum cell. The another advantage of these multilayer structure to increase the output strength. When single layer structure needs a huge number of quantum-cells, at that time, the design-complexity is also maximized. But, in our presented design that kind of recently discussed problem is minimized by using this multiyear crossover technique [19].

Power Model of "QCA"

Power Model of selected "QCA" technology is mainly introduced by Timler and Lent in the year 2002. The power model for every quantum cell depends on the energy flow of quantum-binary-wire and this total energy of any QCA-Component can be calculated through "Hamiltonian Matrix". The "Inter-Cellular Hartree Fock" is utilized in this "Hamiltonian Method" to calculate the power in an array of cells [7], which depends on the polarization of cells, groundstate tunneling-energy (presents between two states) and electrostatic fall-off between two different cells and the kinkenergy. The ultimate power-flow into a quantum cell is an addition of the cell-power-flow and dissipated-power-flow, where the cell-power-flow or P₁ is based on the clock-power or P_{clk}, input-signal-power or P_{in} and Output-signal-power or P_{out} of quantum-cell-wire. The relation among these above powers are clearly represented in this part by using equation 4 and also this part presents the gain-equation of each quantum cell, which is a ratio of P_{out} and P_{in} (is presented in equation 5). The dissipated power of the quantum-cell design depends on the occupied area of the design proportionally. The decrement of area of circuit design is very important to reduce the dissipated power due to the above reason [11].

$$P_1 = P_{in} - P_{out} + P_{clk} (4)$$

Gain = P_{out} / P_{in} (5)

QCA-Pro 1.1-2, a power-analysis tool is used in this work to calculate the power-dissipation of proposed circuit [21]. This power performed at temperature 4 K and 1.0 E_k kink energy, which depends on the temperature of the design. The total power of any QCA design depends on the area and cell-complexity of the design. The area, cell-complexity and temperature-effect of the proposed multilayer reversible design reduction brings less power dissipated value with low kink-energy.

Proposed Designs

In this section, a reversible gate is used to design the proposed "Full-Adder-Subtractor" design with reversible nature in multilayer platform. Then, the used components of different layers are alternated and compared each-other. After this process, the better one is used to convert the proposed singlebit design into multi-bit (4-bit is presented) structure.

Used Reversible Gate

In this proposed multi-output component, modified 3-input Feynman Gate is used as a reversible gate to reduce the design-complexity, area, delay and power dissipation with high output-strength and high temperature-tolerance capabilities. The block of proposed reversible gate is presented below in figure 6 (Let, A, Cin and B are the 3 inputs and X, S/D, Y are the three outputs of proposed reversible gate) with a proper truth-table, given in table 2.



Figure 6. Block-Diagram of the proposed reversible modified 3-input Feynman Gate

	Input		Output		
Α	Cin	В	$\mathbf{X} = \mathbf{NOT} (\mathbf{A})$	S/D = A XOR Cin XOR B	$\mathbf{Y} = \mathbf{B}$
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	0	0	0
1	1	1	0	1	1

Table 2. Truth table of the proposed reversible modified 3-input Feynman Gate

Reversible Multilayer "Full-Adder-Subtractor" Design

As we discussed earlier in this section of this paper that two different Multilayer "Full-Adder-Subtractor" are designed in this work, where the components of 1^{st} and 3^{rd} layer are alternated in these two designs and above reversible gate with a 3-input MG is used here. These two proposed single-bit designs are shown in this portion in figure 7 (a) and (b).



(b)

Figure 7 (a) and (b). Two type of Multilayer Reversible "Full-Adder-Subtractor" design

In the above figure 7 (a) layer 1 presents the carry-output (Cout) and borrow-output (Bout) through 3-input MG based on paper [Ah], layer 3 presents the Sum and Difference output, which is presented as output S and the used transmission line between these two separate layers are specified in layer 2. In the next figure 7 (b), the cell-designs of 1st layer and 2nd layer are exchanged with less-complexity. In this 2nd figure, used reversible gate of layer 1 presents the S-output (Sum and Difference output or S/D) with carry-out (Cout) by using only 12 number of quantum cells and the garbage outputs X and Y are also utilized in this proposed design to get Bout in the 3rd layer by using the 3-input MG same as previous one. If the parameters of the previous two given structures are compared after a proper simulation through "QCA-Designer" and "QCA-Pro" software, then it can be said that the 2nd feature gives better result to reduce

design-complexity, occupied area and power-consumption with very low reduction of average output strength. The outputs are clearly presented in the next section of this paper, where the simulated outputs are parametric comparisons are discussed.

Design of proposed "Full-Adder-Subtractor" Structure After Single-Bit to Multi-Bit Conversion

The 2nd structure of proposed "Full-Adder-Subtractor" circuitry, which is shown in this paper in the previous section, is utilized to design a multi-bit proposed structure in multilayer 3D (3 layers are used) platform and this 3D structure is presented in this portion in figure 8.



Figure 8. Multilayer 4-Bit "Full-Adder-Subtractor" design

The above design of 4-bit "Full-Adder-Subtractor" (figure 8) is mainly based on the hybrid structure of RCA and RBS, which is already discussed previously in this paper. The 1st layer presents the RCA and the 3rd layer presents the RBS. The transmission line between them is placed in 2nd layer. The parametric investigation of this 4-bit proposed design is presented in the next portion of this paper with a simulated outcome and a clear parametric-comparison among the presented design (RCA with RBS) and previously published CLA and CSA [6].

Simulated Outcomes and Comparison

This section presents all the simulation results of previously discussed proposed designs of this paper-work. At first, the

outputs of two presented different Multilayer Reversible "Full-Adder-Subtractor" structures are shown in this section. Then, a comparison table is presented, which proves the advancement of proposed comparatively more acceptable "Full-Adder-Subtractor" design compare to other previouslypublished "Full-Adder-Subtractor" designs from 2017 to till now. After showing the parametric-betterment of proposed circuitry, an outcome of the presented 4-bit structure based on this presented advance single-bit circuitry is given in this portion with a clear comparison with previously published CLA and CSA parametric values. The used parameters to design the selected "QCA" based structure are also presented in this portion in table 3.

e 5. Table of used parameters in selected QCA based simul					
Parameters are used	Values of the parameters				
Cell-Size	18 nm				
Distance between layers	11.5 nm				
Dot-Diameter	5 nm				
Clock-Area (lower)	3.800000e ⁻⁰²³				
Clock-Area (Upper)	9.800000e ⁻⁰²²				
Area of clock-shift	0				
Clock-Amplitude-Factor	2				
Permittivity (relative)	12.90				
Sample-Numbers	50,000				
Convergence-tolerance	0.001				
Maximum interaction of	100				
one sample					

Table 3. Table of used parameters in selected "QCA" based simulation

Results of Proposed Single-Bit Structures

As we discussed above, there are two different Reversible Multilayer circuitries of proposed "Full-Adder-Subtractor" components are simulated thorough "QCA-Designer", figure 9 (a) and (b) presents these two simulated-outputs properly.

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(a)



Figure 9 (a) and (b). Simulated Results of two type of Multilayer Reversible "Full-Adder-Subtractor" design

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If we discuss about the parametric values of these above two presented simulated designs, then it is proved through our work that the 2^{nd} structure can reduce 33 % occupied area, 9.3 % complexity and 33 % power-dissipation with same speed, 0.32 % average output strength reduction and 25 % accuracy increment compare to 1^{st} structure. From this above comparison, it can be also said that the 2^{nd} structure is more acceptable to form an optimized proposed "Full-Adder-Subtractor" design than the 1^{st} one. This more acceptable proposed design is also compared in this work with previously published "Full-Adder-Subtractor" designs, as we discussed earlier and the comparison based on occupied area, delay, cell-complexity, reversibility and used layer-type is presented below in table 4.

Our proposed reversible design is formed in a multilayer platform (3-layers), which is already discussed in this paper previously. But, there is a limitation of output-strength change with temperature increment takes place due to the increment of electron-scattering in high temperature. This proposed reversible multilayer maintains its average output strength up to 4K temperature and this device can give accurate outputs without any malfunction up to 13K temperature. The average output strength change with temperature increment is also presented in this portion in figure 10 by showing a graphical representation.

Table 4. Parametric	Comparison table an	nong differently publishe	ed "Full-Adder-S	Subtractor" design	s in different year

Year	Occupied Area	Cell-Complexity	Delay (ps)	Layer Type	Reversibility
	(µm²)				
2017 [11]	0.6	90	1.5	Multilayer	Irreversible
2018, June [12]	0.14	121	0.5	Single Layer	Reversible
2018, September	0.04	49	0.5	Multilayer	Irreversible
[13]					
2019 [14]	0.039	48	0.75	Single Layer	Reversible
2020 [15]	0.03	38	0.5	Multilayer	Irreversible
Proposed	0.02	29	0.5	Multilayer	Reversible



Results of Proposed Multi-Bit Structure

This section presents the simulated output of multibit (4-bit) multilayer "Full-Adder-Subtractor" design by using the above proposed advanced single-bit structure and figure 11 is used to present the simulation result.

Figure 10. The graphical representation of average output strength changes with temperature increment in the



Figure 11. Simulated Result of Multilayer 4-bit "Full-Adder-Subtractor" design

In that above figure only the last bit of 4-bit structure is shown with the proper ultimate carry-output, when the A3 is 1 and B3 is 0. In this A3-B3 combination if the carry-out of previous bit is 1, then the next carry-out is also 1, the

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sum/difference (S3) output becomes 0 and the ultimate borrow out is 0 in this result. As we discussed previously in this paper that this proposed multi-bit design is compared with previously published CLA and CSA design, the comparison table is shown in this part as table 5. A graphical representation of the area-latency-cost-comparison based on the given table 5 is also shown over here in figure 12.



Figure 12. The graphical representation of the area-latencycost-comparison based on the given table 5

Table 5. Parametric Comparison table among previously published CLA, CSA [6] and proposed 4-bit "Full-Adder-Subtractor"

Adder-Type	Area-Occupation (µm ²)	AUF	Complexity	Latency (ps)	Layer- type	Design-Cost (Area X Latency ²)
CLA	0.92	11.5	777	2.75	Multilayer	6.95
CSA	0.66	9.42	696	2.25	Coplanar	3.34
Proposed 4-bit Multilayer "Full- Adder-Subtractor"	0.12	2.116	175	1.5	Multilayer	0.27

That above structure proves that, the proposed 4-bit 3-layered adder circuitry with ripple-borrow-out not only reduce the occupied area, delay and cell-complexity, but also reduce the area-utilization-factor (AUF) [22] and cost of the design, which depends on area and latency or delay of the design, with 1.2 nW areal power-dissipation [23]. The equation of area-utilization-factor is also given below as eq. 6.

$$\begin{split} AUF = & [[(N_1 * M_1) + \{(N_1 - 1) * P_1\}] * [(N_2 * M_2) + \{(N_2 - 1) * P_2\}]] / (N * M_1 * M_2) \end{split}$$

In the above equation,

- N_1 = Number of used cells horizontally of proposed design
- N_2 = Number of used cells vertically of proposed design
- N = Number of total used cells
- M_1 = Length of each cell
- M_2 = Width of each cell
- P_1 = Distance between two cells horizontally
- $P_2 = Distance$ between two cells vertically

Conclusion

This paper mainly focusses to optimize the occupied area, power-dissipation and delay of a "Full-Adder-Subtractor" design with 100 % accuracy, temperature-tolerance up to 13 K and an acceptable average-output-strength compare to other previously discussed similar designs and reversible gate with less cell-complexity is applied in this work in multilayer 3D "QCA" platform to achieve the above aims of this paper, where electro-spin criterion takes place. 33 % area reduction and 23 % cell-complexity reduction than a 2019's published similar component [15] is possible in this proposed one bit "Full-Adder-Subtractor" design. Multilayer multi-bit (up to

4-bit) design formation using the proposed reversible multilayer single-bit structure is also shown in this paper, where a RCA is presented with ripple-borrow-output and this feature is more advance to reduce the area, delay, design-cost and cell-complexity with less power-dissipation compare to previously published 4-bit CLA and CSA design [6]. This design can reduce 81 % of area-occupation, 77 % AUF, 74 % cell-complexity, 33 % delay and 91 % design-cost compare to the given advanced 4-bit adder design (CSA) in a previous work. This multi-bit design in multilayer platform can be improved more in future with proper hardware verification and fabrication process.

References

- 1. Mersede Zahmatkesh, Sepehr Tabrizchi, Somaye Mohammadyan, Keivan Navi1, Nader Bagherzadeh (2019). Robust Coplanar Full Adder Based on Novel Inverter in Quantum Cellular Automata. *International Journal of Theoretical Physics* 58:639-655.
- C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernstein (1993). Quantum Cellular Automata. Nanotechnology 4:49
- 3. Niemier MT (2000). Designing digital systems in quantum cellular automata. *University of Notre Dame*.
- 4. Kim K, Wu K, Karri R (2005). Towards designing robust QCA architectures in the presence of sneak noise paths. *In: Proceedings of the Conference on Design, Automation and Test in Europe* 2:1214–1219.
- 5. Azghadi MR, Kavehie O, Navi K (2012). A novel design for quantum-dot cellular automata cells and full adders. *arXiv*: 1204.2048.

An Interdisciplinary Journal

Article Received: 16th October, 2020; Article Revised: 30th December, 2020; Article Accepted: 08th January, 2021

- 6. Sarvarbek Erniyazov, Jun-Cheol Jeon (2019). Carry save adder and carry look ahead adder using inverter chain based coplanar QCA full adder for low energy dissipation. *Microelectronic Engineering* 211:37-43.
- 7. Subhash S. Pidaparthi, Craig S. Lent (2018). Exponentially Adiabatic Switching in Quantum-Dot Cellular Automata. *Journal of Low Power Electronics and Applications* 8:1-15.
- 8. Saeed Mirzajani Oskouei, Ali Ghaffari (2019). Designing a new reversible ALU by QCA for reducing occupation area. *The Journal of Supercomputing* 75(8):5118-5144.
- 9. Kianpour M, Sabbaghi-Nadooshan R (2017) Novel 8bit reversible full adder/subtractor using a QCA reversible gate. *J Comput Electron* 16(2):459–472
- 10. Taherkhani E, Moaiyeri MH, Angizi S (2017) Design of an ultra-efficient reversible full adder-subtractor in quantum-dot cellular automata. *Optic* 142:557–563
- 11. Barughi YZ, Heikalabad SR (2017) A three-layer full adder/subtractor structure in quantum-dot cellular automata. *Int J Theor Phys* 56(9):2848–2858
- Firdous Ahmad, Suhaib Ahmed, Vipan Kakkar, Mohiuddin Bhat, Ali Newaz Bahar, Shahjahan Wani, (2018) Modular Design of Ultra-Efficient Reversible Full Adder-Subtractor in QCA with Power Dissipation Analysis. Int J Theor Phys. https://doi.org/10.1007/s10773-018-3806-3.
- Md. Abdullah-Al-Shafi and Ali Newaz Bahar (2018) An Architecture of 2-Dimensional 4-Dot 2-Electron QCA Full Adder and Subtractor with Energy Dissipation Study. Active and Passive Electronic Components, *Hindawi* 5062960: 1-10. https://doi.org/10.1155/2018/5062960.
- Moein Sarvaghad-Moghaddam and Ali A. Orouji (2019) New symmetric and planar designs of reversible full-adders/subtractors in quantum-dot cellular automata. *Eur. Phys. J. D* 73: 125. https://doi.org/10.1140/epjd/e2019-90315-x.
- 15. Mostafa Sadeghi, Keivan Navi, Mehdi Dolatshahi

(2020) Novel efficient full adder and full subtractor designs in quantum cellular automata. *The Journal of Supercomputing* 76:2191–2205. https://doi.org/10.1007/s11227-019-03073-4.

- 16. Seyed-Sajad Ahmadpour, Mohammad Mosleh, Saeed Rasouli Heikalabad (2020) The design and implementation of a robust single-layer QCA ALU using a novel fault-tolerant three-input majority gate. *The journal of Supercomputing*. https://doi.org/10.1007/s11227-020-03249-3
- 17. Jeyalakshmi Maharaj, Santhi Muthurathinam (2019) Effective RCA Design using Quantum dot Cellular Automata. *Microprocessors and Microsystems*. https://doi.org/10.1016/j.micpro.2019.102964
- Noel D'Souza, Jayasimha Atulasimha, Supriyo Bandyopadhyay (2012) An Energy-Efficient Bennett Clocking Scheme for 4-State Multiferroic Logic. *IEEE Transactions on Nano Technology*. DOI: 10.1109/TNANO.2011.2173587.
- 19. Waje MG, Dakhole P (2013) Design implementation of 4-bit arithmetic logic unit using quantum dot cellular automata. *IEEE, IACC*:1022-1029.
- 20. Prashant. R. Yelekar, Sujata S. chiwande (2011) Introduction to reversible logic gates & application. *NCICT, IJCA*:5-9.
- 21. Ismail Gossoumi, Lamjed Touil, Bouraoui Ouni, Abdellatif Mtibaa (2019) An Ultra-Low Power Parity Generator Circuit Based On QCA Technology. Journal of Electrical and Computer Engineering: 1-8.
- 22. Mukesh Patidar, Namit Gupta (2020) An efficient design of edge-triggered synchronous memory element using quantum dot cellular automata with optimized energy dissipation. *Journal of Computational Electronics* 19: 529–542.
- J. Timler, and C. S. Lent (2002). Power gain and dissipation in quantum-dot cellular automata. J. Appl. Phys. 91:823–31.