Low Leakage Approximate multiplier design for high Performance Error Tolerant Applications

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ABSTRACT

Power dissipation has become a major concern in VLSI circuit design with the rapid launch of battery powered applications. In high-performance constructions, the leakage component of power consumption is comparable to the switching component. This percentage increases as the technology scales unless effective leak control techniques are in place. In the case of fault-tolerant applications it is also not necessary to adhere to the exact calculation method. Therefore, an approximate multiplier of 8 x 8 is developed in this article using several proposed techniques to reduce leakage power such as MTCMOS, DUAL-Vt, and LECTOR. All of the above techniques are simulated with a tanning tool using 90 nm technology.

Keywords

High-performance constructions , Leakage current, power dissipation, Dynamic power,MTCMOS,Dual-Vt,LECTOR

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Introduction

Approximate Computing (AC) is a wide range of techniques that reduce the precision of a computation to improve performance, power, and / or other quality metrics. AC takes advantage of the fact that some critical applications like machine learning and media processing do not require accurate results to be useful. For example, we can use a lower resolution image encoder in applications that do not require high quality images.

Technology Scaling

Power dissipation is an important consideration in VLSI CMOS circuit design. High power consumption leads to reduced battery life in battery-powered applications and affects reliability, packaging and cooling costs. The main sources of power dissipation are: 1) capacitive power dissipation due to the charging and discharging of the load capacitor; 2) short-circuit currents due to the presence of a conductive path between the supply voltage and earth for the short time during the transition of the halogen; and 3) the leakage current. The leakage current consists of reverse bias diode currents and currents below the threshold. The first is due to the charge stored between the drain and the bulk of the active transistors, while the second is due to carrier diffusion between the source and drain of the OFF transistors.

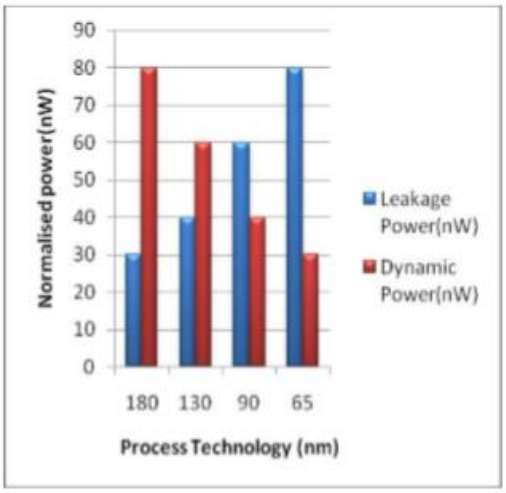

Fig. 1. Leakage and Dynamic power consumption with technology scaling

Approach To Analyse

The market demand and efficient portable electronic equipment have pushed the industry to produce circuit designs operating at low voltage (LV) for low power (LP) consumption. Reducing the supply voltage reduces the dynamic power quadratic ally and leakage power linearly to the first order. Hence, supply voltage scaling has remained the major focus of the low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor (i.e. subthreshold region). One of the main contributors for the static power consumption is sub-threshold leakage current, the drain to source current when the gate voltage is smaller than the threshold voltage. As the technology feature size shrink sub threshold leakage current increases exponentially due to the decrease of threshold voltage. According to the International Technology Roadmap for Semiconductors (ITRS) [1]. However, reduction in supply voltages requires

that threshold voltage (VT) also be scaled down proportionally. Devices with lowered VT would dissipate more leakage power in standby mode, dominated by sub-threshold leakage current. This can be very significant in burst-mode type electronic circuits. Three main components of leakage mechanisms in scaled devices can be readily identified as Gate leakage, sub-threshold leakage and Band-To-Band Tunnelling (BTBT) leakage [2].

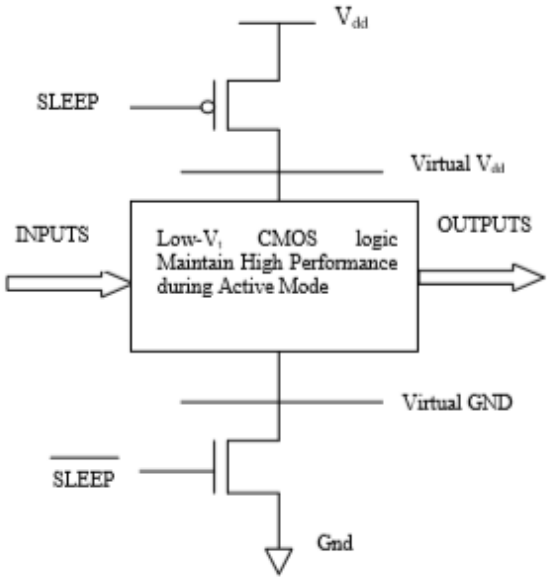

Fig 2: General MTCMOS circuit architecture

Multi-threshold CMOS (MTCMOS) is a design technique in which high threshold sleep transistors are connected between the logic circuit and power or ground, thus creating a virtual supply rail or virtual ground rail, respectively. The low threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path [4],[5]. There are methods high threshold voltage (HTV) is assigned to transistors of some gates in the non-critical paths while specifying the low-threshold voltage for the gates in the critical path. In this technique, no additional transistors are required as in the case of multithreshold voltage technique. Reduction of static power is achieved while maintaining the same performance as single threshold voltage circuit [6], [7].

Existing Method

One of the main contributors for the static power consumption is sub-threshold leakage current, the drain to source current when the gate voltage is smaller than the threshold voltage. As the technology feature size shrink subthreshold leakage current increases exponentially due to the decrease of threshold voltage. According to the International Technology Roadmap for Semiconductors (ITRS) [1], leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink to nanometer regime in deep submicron technologies. The method existing right now consists of various methods & techniques which are used for reducing the leakage power in VLSI circuits.

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. Low, normal and high threshold voltage transistors are used to design a CMOS circuit in this technique. With the scaling of CMOS technology, Supply and threshold voltages are reduced. Sub threshold leakage current increases exponentially with lowering of threshold voltage.

Proposed Method

The memory in various components is designed to process at high performance speed. These memory devices also having the challenge to reduce the delay to the decoder as it will improve the overall processing of the system. CMOS is one such device that requires reducing the delay. The optimization of a VLSI design can be done by reducing the transition of information to the decoder.[8]The proposed approach involves two main steps. In the first case, the lossy compression is done through logical clustering. These steps and the variable compression method are described below. Logical Compression: The design of parallel multiplication is usually divided into three successive stages: Adders for Partial Product Formation, Accumulation and Transport Propagation In a multiplier (N × N), N2 AND gates are used in parallel to generate the partial product bit matrix. This matrix is then accumulated per column to produce the final product using carry propagation adders. The proposed approach starts with the generation of all partial products using the same number of AND gates, similar to conventional multiplication. Before proceeding with the accumulation step, the number of bits in the partial product matrix is reduced by performing a lossy logic compression. The aim is to reduce the number of rows in the partial product matrix and thus obtain material with low complexity before proceeding with the accumulation. Commutative reassignment: The logical compression step reduces the number of sub-terms of the product. This reduction can be used to reduce the number of lines before the accumulation step. This can be achieved by reallocating the terms of the partial product based on the commutative property of the bits; H. Bits of the same weight are collected in the same column. A partial product is generated using an AND gate, and the outputs generated by the gate are then approximated using an array of half OR gates. A reduced set of preprocessed partial product matrix can thus be accumulated by applying any practical multiplication scheme such as the save-carry table, Wallace and the dadda tree. In theory, an OR gate with two inputs is sufficient to sum two bits, i.e. '0' + '1' = '1' + '0' = '1' '0'OR'1' = '1' OR ' 0 '=' 1 'and also' 0 '+' 0 '=' 0'OR'0 '=' 0 '. However, the OR gate does not provide an exact sum when both inputs are high, i.e. H. "1" + "1" = "1" OR "1", the adder returns "10" and the OR outputs "

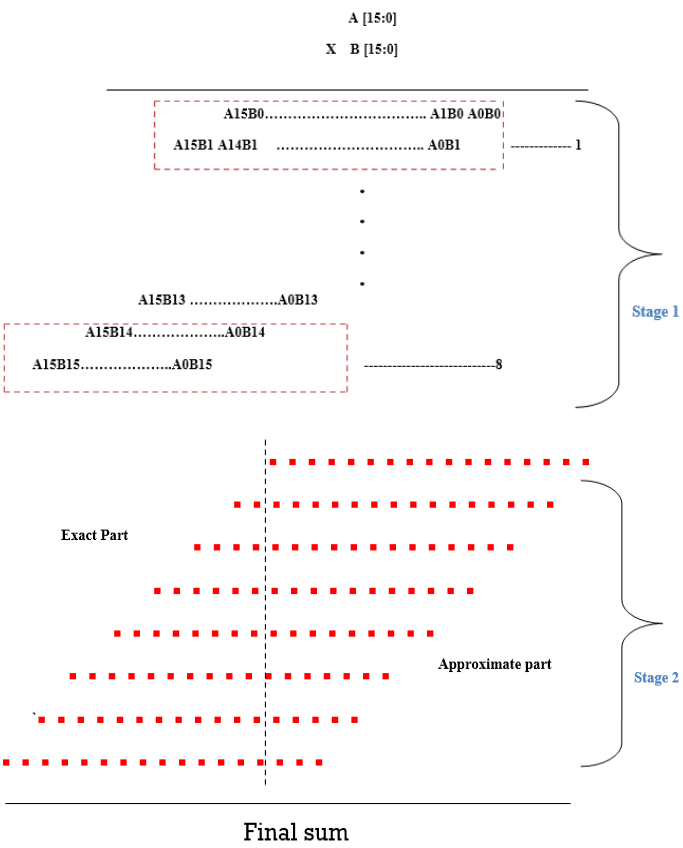

Fig 3 : Proposed approximation Algorithm

For the proposed approximate multiplier, the techniques that are applied in the existing multiplier are applied to reduce the static power consumption, which is the dominant in lower technologies. Hence along with approximation, we are also implementing the Leakage power techniques such as Modified MTCMOS, DUAL-VT and LECTOR techniques that are used in the existing multiplier to reduce the leakage power which is result of drastic scaling.

Results

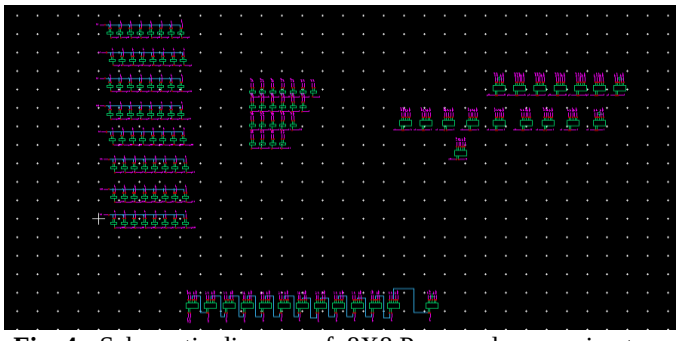

Fig. 4 : Schematic diagram of 8X8 Proposed approximate multiplier using MTCMOS technique

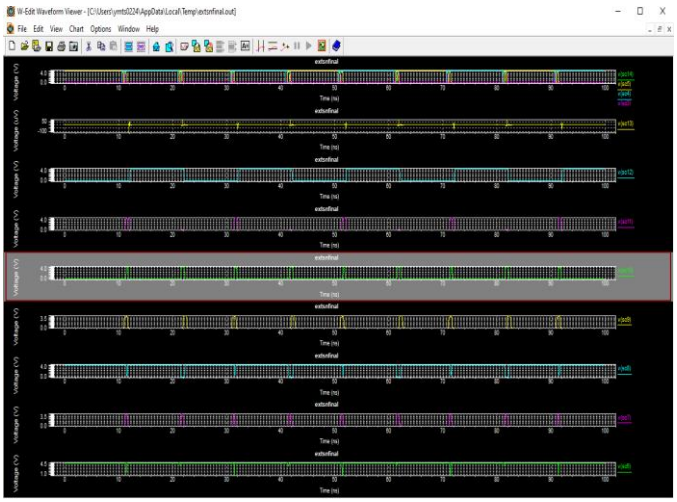

Fig. 5: Waveform of 8X8 Proposed approximate multiplier using MTCMOS technique

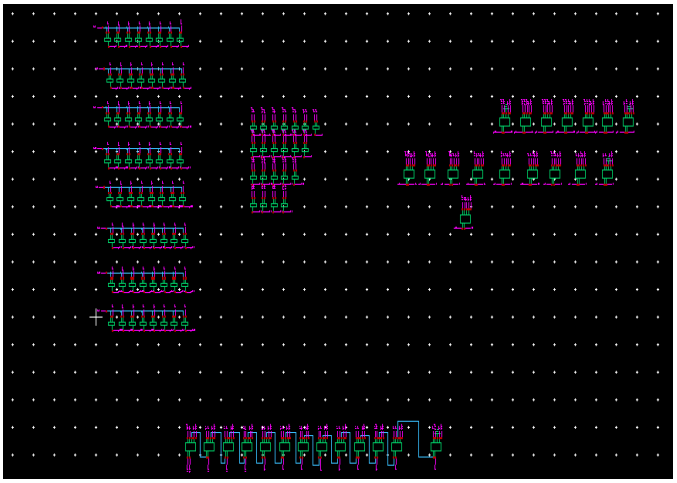

Fig. 6: Schematic diagram of 8X8 Proposed approximate multiplier using Dual Vt technique

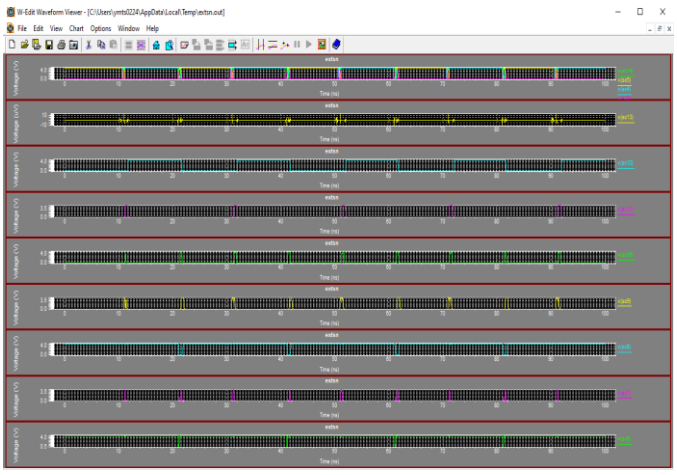

Fig. 7: Waveform of 8X8 Proposed approximate multiplier using Dual Vt technique

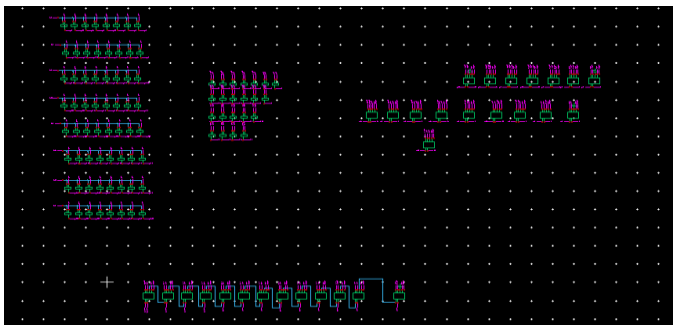

Fig. 8 Schematic diagram of 8X8 Proposed approximate multiplier using Lector technique

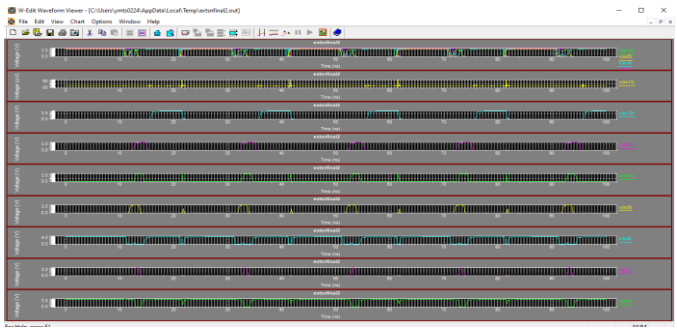

Fig. 9: Waveform of 8X8 Proposed approximate multiplier using Lector technique

Name of technique	Area(transistor count)	Delay(ns)	Power(mw)
Existing multiplier using Dual Vt	2008	1.21	44.8
Existing multiplier using Lector	2120	2.02	200
Existing multiplier using MTCMOS	2120	1.32	55
Proposed multiplier using Dual Vt	1386	1.04	29
Proposed multiplier using Lector	1446	1.16	117
Proposed multiplier using MTCMOS	1446	1.12	33.2

Fig.10 Comparison between existing and proposed multiplier

Conclusions

In this paper, an approximate 8x8 approximate multiplier is designed with different leakage power reduction techniques like Multi-Vt, Dual-Vt, LECTOR to improve the performance in terms of delay, area and power. Simulation results in tanner tool show that the proposed method shows better results in terms of power, area and delay reports when compared to existing multiplier.

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